EXHIBIT Q

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PART II of III

FOCUS ON Verigy vs. STS

On August 22, 2007 Verigy filed a Complaint, in the U.S. District Court for the Northern District of California, against a former employee, Romi Omar Mayder, his brother Wesley Mayder and their start-up company Silicon Test Systems. Verigy's complaint alleged "breach of contract, trade secret misappropriation and intentional interference with prospective economic advantage and unjust enrichment."

On August 24, 2007, the Judge hearing this case, Ronald M. Whyte, issued a temporary restraining order – based on evidence presented by Verigy the court said "strongly suggested that Mayder had transmitted project documents he had authored at Verigy to a third party, Bob Pochowski, for the purpose of using those documents to launch his own independent business – against STS. That order remained in effect until the preliminary injunction was issued on February 29, 2008.

Editor's Note: Most of the following was sourced from the heavily redacted 'Public Version' of Judge Whyte's order.

Verigy's Complaint sought a "preliminary injunction" based largely on its "trade secret misappropriation" claim. Under California Law a 'trade secret' can be any information, including a formula, pattern, compilation program, device, method, technique, or process that:

(1) Derives independent economic value, actual or potential, from not being generally known to the public or to other persons who can gain economic value from its disclosure or use: and,

(2) Is the subject of efforts that are reasonable under the circumstances to maintain its secrecy.

Romi Mayder had been employed by Verigy and its predecessors – HP and Agilent – from 1998 until September 21, 2006. During the latter part of his employment at Verigy Mayder had worked on several projects there involving the development of methods to 'fan-out' of FLASH memory tester resources to expand the number of chips that could be tested in parallel.

According to Mayder, while still employed at Verigy, the approach that Mayder had been working on was canceled, so he decided to start his own company to commercialize that technology, which he felt Verigy had abandoned. He registered the Web domain name *silicontests.com* on June 15, 2006. At that time he also contacted Bob Pochowski to explore his interest in forming a company with him, presumably as both an investor and a technology resource.

Pochowski had founded NOR FLASH tester maker Versatest in 1988 with Keith Armstrong. In 1994 they sold the company to HP for a reported $14 million, which they effectively split. He served as head of HP's and Agilent's memory tester groups at various times and eventually became a technical consultant to the company when it became Verigy.

According to court documents Mayder had transmitted a number of documents to Pochowski at that time, These included a draft RFQ – which he also sent to Honeywell for a quote – for a semiconductor chip containing an unspecified number of solid-state switches and a spread sheet of NAND FLASH wafer sort requirements for five of Verigy's customers. He also sent Pochowski a PowerPoint presentation titled "Tester Expander".

(Verigy asserts these actions were in direct contradiction of a confidentiality and proprietary development agreement Mayder had signed as part of his employment at Verigy, which is dated just one month before he sent these documents to Pochowski.)

Sometime after July 2006 Pochowski agreed to became Mayder's business partner, along with Mayder's brother Wesley. However, he left STS in December 2006 after a disagreement over each partner's ownership of STS. According to court documents he became "the source of information upon which Verigy bases its allegations."

STS planned to base its business on a family of products it called "Flash Enhancer" ICs. That according to information on its presently shutdown Web site It describes them as "uniquely designed devices to optimize the parallelism of already installed ATE test cells supporting the full array of today's high volume memory devices, FLASH, DRAM, and MCPs."

It further claimed that "The use of our integrated circuit products will enable an existing wafer sort test cell to test up to 2X or 4X the existing number of DUTs. For example our integrated circuit products transform a 2 TD [Touch Down] test cell into a 1TD test cell with minimal test time overhead. They will also enable an existing final test cell to test up to 4X or 8X the existing number of DUTs. For example our integrated circuit products transform a 256 in parallel test cell into a 512 in parallel test cell."

STS originally had targeted its first Flash Enhancer product at NAND FLASH makers but did not find any interest "because the potential customers decided to manufacture their own resource sharing circuits." It then turned to NOR FLASH makers and found interest in its approach from Intel and Spansion. (STS argues that it had to redo [the Verigy design] to meet those customers' NOR test requirements.)

However the court was not convinced as Verigy had presented evidence that many of the features of the 'new Flash Enhancer' are relatively unchanged from what they were when Mayder was still at Verigy. However, the court also concluded that Verigy had not presented evidence that these companies' requirements on which the present version of the Flash Enhancer is based were originally collected by Verigy.

The court concluded that STS's product, though now based on NOR rather than NAND test "is substantially based on Verigy's trade secrets. However it, at the very least, has relatively significant changes from what was developed at Verigy, including features added based on customer requirements that were not originally collected by Verigy." Accordingly the court said it "cannot say the Flash Enhancer is solely an embodiment of Verigy's trade secrets."

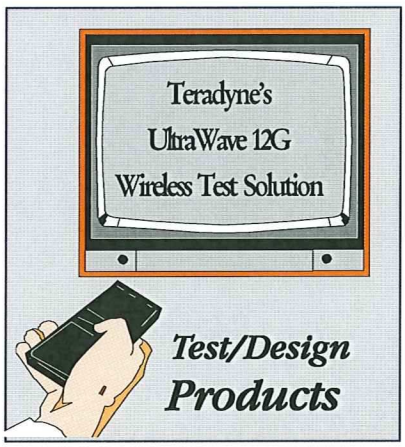
It also concluded that "it appears that Mayder, given his skill and experience, could have eventually developed the Flash Enhancer'without benefit of any Verigy trade secrets by referring to publicly-available references regarding fan-out technology."

Finally, the court concluded that STS had obtained a 'head-start' on the development of its Flash Enhancer product [as a result of Mayder' work at Verigy.] It decided that "Accordingly, it would enjoin STS for a period of five months from the date of its order [presumably until August 1) from marketing, distributing, selling, licensing, leasing, transferring or disposing of its, Flash Enhancer, and any product based on Flash Enhancer"

However, its not clear that this is really the end of this story. The Judge accepted Verigy's motion to "strike STS's affirmative defenses. STS was given 20 days to present "facts to support their affirmative defenses." In addition he required STS to show cause why they should not be held in contempt of the initial injunction.

A hearing on both of these matters is scheduled for April 11.

So, stay tuned!

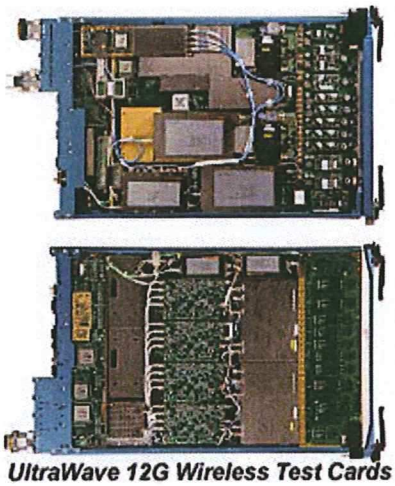


Teradyne introduced its new *UltraWave* test instrument for its *UltraFLEX* test platform. It offers 12 GHz source and measurement performance, with greater parallel test efficiency and covers the entire spectrum of current and emerging connectivity and cellular technologies, according to the company. It also said it has already has received orders from "multiple customers" for the product with Broadcom the first customer to take delivery of the instrument.

UltraWave's unique universal port architecture provides 12 GHz source and measure with uniform test capability on every port. UltraWave can be configured with up to 64 universal RF ports per instrument set and multiple instruments per system, easily providing parallel octal site test without needing complex DIB circuitry for high port count devices, such as WEDGE transceivers and 802.11n applications.

UltraWave incorporates Teradyne's patent-pending *TVS* synthesizer technology that provides fast settling time to 0.07dB within 1 millisecond and superior phase noise. Teradyne said that "UltraWave delivers DSP per receiver with calculations performed in less than 20 microseconds.

UltraWave leverages Teradyne's UltraFLEX system architecture that incorporates *Sync-Link* test technology for pattern-controlled instrument set-up at device clock speed, *System Broadcast* for faster, high-efficiency instrument set up



UltraWave 12G Wireless Test Cards

Also a Background DSP environment puts data moves and analysis in the background of program execution. The result is the highest parallel efficiency for RF multi-site test.

The UltraFLEX system's *IG-XL* software operating system provides fast program development and automatic conversion of programs from single-site to multisite test. Graphical on-screen displays, like Smith charts, vector scopes, Constellation, and EVM simplify program analysis, debug and correlation to bench instrumentation for faster time to market. Variables and debug tools are available on a site-by-site basis and provide the ability to control all sites simultaneously.

Features & Specifications

- Up to 96 universal RF ports per instrument set
- Multiple instrument sets/system
- 50 MHz to 12 GHz Source and Measure
- Parallel stimulus and measure capability
- Noise source per port
- Vector network analyzer
- DSP per receiver
- Integrated AWG for modulated signal generation
- Integrated Low Phase Noise Reference Source
- 4 DUT LO source pins (50 MHz to 6 GHz)
- 4 DUT Reference source pins (8 MHz to 100 MHz)

Credence DD1096-32 Diamond Instrument

Credence Systems introduced its DD1096-32 digital instrument - an update of its previous DD1096-16 instrument increasing its parallel vector memory to 32M - for its Diamond test platform, at SEMICON China last month. Using the 96 channel DD1096-32 within the 10-slot Diamond 10 offers customers up to 768 channels, each with 32M of parallel vector memory depth.

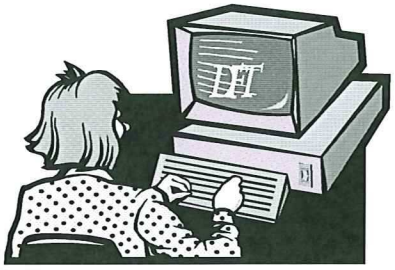
The DD1096-32 also enables up to 256 scan chains and over 77G of scan vectors. For massive multisite use in high-mix, high-volume production applications the 40-slot Diamond 40 with DD1096-32 scales up to 3072 channels with up to 1024 scan chains and over 309G scan vectors.

The company said, "The DD1096-32 instrument's larger memories also provide enhanced test and debug capability with full memory depth deep fail and data capture which allows customers to quickly and confidently test complex, highly integrated devices in a single pass.

At less than US$600/pin, the fully featured digital instrument offers the industry's best combination of performance and density in an air-cooled test system the size of a large desktop computer."

Each of the 96 digital channels offers parametric measurement units, independent timing, formats and levels that enable flexible edge placement and digital signal creation for complex tests. Its 100MHz pattern sequencer can provide 200MHz clocks and drive data rates up to 200Mbps.

The DD1096-32 comes with a flexible instruction set to support conventional functional tests, along with STIL-based EDA integration for structural test methods. It can handle any combination of input or output chains, useful for built-in self test (BIST) enabled devices. Moreover, two bits per scan output cycle allows masking of failing scan cells to improve debug productivity



Pintail and Salland Join on Adaptive Test

Pintail Technologies and Salland Engineering (Zwolle, Netherlands) have partnered to share technology roadmaps and product integration plans for Adaptive Test solutions, as well as conducting joint marketing on a worldwide basis. The companies said that "Numerous customers of both company's products have recognized the synergistic fit between the product lines and have encouraged the companies to collaborate more closely."

Taylor Scanlon, president/CEO of Pintail said, "Salland's *SE-PROBE* is a comprehensive real time wafer mapping and dynamic test cell controller on the market today. Its solutions for Adaptive Test are complementary to Pintail's and expand our solutions for test optimization and dynamic parts average testing (DPAT.)

The companies plan to closely integrate *SEDana* (Salland's tool for statistical analysis of ATE test data) as the off-line analysis tool used to predict the performance of Pintail's *SwifTest-MX* when used for test time reduction and *SwifTest-AQ for* adaptive quality improvement. In addition, test floor managers will now be able to integrate the real-time OEE capabilities of Pintail's *TestScape* system with the functionality of Salland's real time test cell controller SEPROBE. "TestScape provides test floor managers a real-time dashboard to monitor multiple test floors and many brands of ATEs," stated Keith Arnold, Pintail's Chief technical Officer.

"By adding Salland's SE-PROBE as the test cell controller, test floors will be able to improve the data integrity of the enormous volumes of test results being monitored. SEPROBE also provides sophisticated capabilities to reduce retest costs, improve contact life cycle management, and other on-line test optimization with Avago Technologies' algorithms.

Pintail said it will incorporate advanced outlier detection algorithms developed by Avago Technologies into its SwifTest commercial software offerings. It said that Avago worked closely with Pintail over the past 12 months as Pintail re-architected SwifTest to accommodate more sophisticated and general purpose sets of data models and program interfaces. "Users will also be able to add their own proprietary algorithms to SwifTest for performing on-line test time reduction or quality improvement," Pintail said.

LogicVision Stock Reverse Split 1:2.5

LogicVision executed a reverse split of its common stock at a ratio of 1-for-2.5 shares effective on March 12, 2008. The reverse split was required for it to maintain its listing on the Nasdaq marker. LogicVision's common stock began trading at that time on a reverse split basis under the symbol "LGVND" for a period of 20 trading days - until April 11, 2008. Thereafter, it will resume trading under its original symbol "LGVN."

The reverse stock split will reduce the number of outstanding shares of LogicVision's common stock from approximately 24 million shares to approximately 9.7 million shares.

EDA STOCKS

COMPANY	Ticker	Close 03/31	Change Month	52 Week High	52 Week Low
Cadence	CDNS	$10.68	0.6%	$24.90	$9.89
LogicVision	LGVN	$1.59	-9.1%	$3.00	$1.20
Mentor	MENT	$8.83	-3.0%	$17.38	$7.51
Synopsys	SNPS	$22.71	-2.2%	$29.11	$21.13
Avg. Change			-3.4%		